What is claimed is:

1. A semiconductor substrate, comprising:

a substrate of a first conductivity type, having a first main surface and a second main surface which are opposed to each other;

an impurity diffusion layer of a second conductivity type different from said first conductivity type, being formed in said first main surface by diffusing an impurity; and

an impurity diffusion region of said second conductivity type, being formed partially in said second main surface by diffusing an impurity, having a bottom surface reaching said impurity diffusion layer and surrounding a portion of said substrate which has said first conductivity type in a plan view,

wherein said portion surrounded by said impurity diffusion region is defined as an element formation region.

2. The semiconductor substrate according to claim 1, wherein

the thickness of said impurity diffusion layer is almost equal to the depth of said impurity diffusion region from said second main surface.

3. The semiconductor substrate according to claim 1, wherein

the impurity concentration distribution of said impurity diffusion layer from said first main surface towards the inside of said substrate is almost equal to the impurity concentration distribution of said impurity diffusion region from said second main surface towards the inside of said substrate.

4. The semiconductor substrate according to claim 1, wherein

the thickness of said impurity diffusion layer is thinner than the depth of said impurity diffusion region from said second main surface.

5. A semiconductor device, comprising:

a semiconductor substrate which comprises (a) a substrate of a first conductivity type, having a first main surface and a second main surface which are opposed to each other, (b) an impurity diffusion layer of a second conductivity type different from said first conductivity type, being formed in said first main surface by diffusing an impurity and (c) an impurity diffusion region of said second conductivity type, being formed partially in said second main surface by diffusing an impurity, having a bottom surface reaching said impurity diffusion layer and surrounding a portion of said substrate which has said first conductivity type in a plan view, said portion surrounded by said impurity diffusion region being defined as an element formation region; and

a first impurity region of said second conductivity type, being formed partially in said second main surface in said element formation region.

6. The semiconductor device according to claim 5, further comprising

a second impurity region of said first conductivity type, being formed partially in said second main surface in said first impurity region,

wherein said first impurity region serves as a base of a transistor,

said second impurity region serves as an emitter of said transistor, and

said impurity diffusion layer serves as a collector of said transistor.

7. The semiconductor device according to claim 6, further comprising

a gate electrode formed on said second main surface with a gate insulating film

interposed therebetween above said first impurity region positioned between said second impurity region and a portion of said substrate which has said first conductivity type.

8. The semiconductor device according to claim 6, further comprising

a local lifetime region formed in said portion of said substrate which has said first conductivity type.

9. The semiconductor device according to claim 8, wherein said local lifetime region has a first local lifetime region formed by implanting proton into a substantially middle region, with respect to a film thickness direction, of said portion of said substrate which has said first conductivity type.

10. The semiconductor device according to claim 9, wherein said local lifetime region further has a second local lifetime region formed by implanting helium into a deep region of said portion of said substrate which has said first conductivity type, said deep region being nearer to said impurity diffusion layer than said first local lifetime region.

11. The semiconductor device according to claim 6, further comprising:

a first main electrode formed on said first main surface, being in contact with said impurity diffusion layer; and

a second main electrode formed on said second main surface, being in contact with said first and second impurity regions.

12. A semiconductor device comprising:

a semiconductor substrate which comprises (a) a substrate of a first conductivity

type, having a first main surface and a second main surface which are opposed to each other, (b) an impurity diffusion layer of a second conductivity type different from said first conductivity type, being formed in said first main surface and serving as a collector of a transistor, and (c) an impurity diffusion region of said second conductivity type, being formed partially in said second main surface, having a bottom surface reaching said impurity diffusion layer and surrounding a portion of said substrate which has said first conductivity type in a plan view, said portion surrounded by said impurity diffusion region being defined as an element formation region;

a first impurity region of said second conductivity type, being formed partially in said second main surface in said element formation region and serving as a base of said transistor;

a second impurity region of said first conductivity type, being formed partially in said second main surface in said first impurity region and serving as an emitter of said transistor;

a gate electrode formed on said second main surface with a gate insulating film interposed therebetween above said first impurity region positioned between said second impurity region and a portion of said substrate which has said first conductivity type; and

a first local lifetime region formed by implanting protons into a substantially middle region, with respect to a film thickness direction, of said portion of said substrate which has said first conductivity type.

13. The semiconductor device according to claim 12, further comprising a second local lifetime region formed by implanting helium into a deep region of said portion of said substrate which has said first conductivity type, said deep region being nearer to said impurity diffusion layer than said first local lifetime region.

14. A method of manufacturing a semiconductor substrate, comprising the steps of:

(a) preparing a substrate of a first conductivity type, having a first main surface and a second main surface which are opposed to each other;

(b) forming an impurity diffusion layer of a second conductivity type different from said first conductivity type by diffusing a first impurity into said substrate from said first main surface; and

(c) forming an impurity diffusion region of said second conductivity type by diffusing a second impurity into said substrate from part of said second main surface, to have a bottom surface reaching said impurity diffusion layer and surround a portion of said substrate which has said first conductivity type in a plan view,

wherein said portion surrounded by said impurity diffusion region is defined as an element formation region.

15. The method according to claim 14, wherein

said step (b) has the steps of:

(b-1) forming a film containing said first impurity on said first main surface; and

(b-2) diffusing said first impurity into said substrate from said film.

16. The method according to claim 14, wherein

said step (c) has the steps of:

(c-1) forming a first film partially on said second main surface;

(c-2) forming a second film containing said second impurity on said second main surface to cover said first film; and

(c-3) diffusing said second impurity into said substrate from said second film.

17. The method according to claim 14, wherein

said step (b) has the steps of:

(b-1) forming a first film containing said first impurity on said first main surface; and

(b-2) diffusing said first impurity into said substrate from said first film,

said step (c) has the steps of:

(c-1) forming a second film partially on said second main surface;

(c-2) forming a third film containing said second impurity on said second main surface to cover said second film; and

(c-3) diffusing said second impurity into said substrate from said third film, and

said steps (b-2) and (c-3) are executed in the same process.

18. The method according to claim 14, further comprising the steps of:

(d) forming a first oxide film entirely on said first main surface and a second oxide film entirely on said second main surface by oxidizing a surface of said substrate;

(e) removing the whole of said first oxide film; and

(f) removing part of said second oxide film,

wherein said steps (d) to (f) are executed before said steps (b) and (c),

said step (b) has the steps of:

(b-1) forming a first film containing said first impurity on said first main surface; and

(b-2) diffusing said first impurity into said substrate from said first film, and

said step (c) has the steps of:

(c-1) forming a second film containing said second impurity on said second main surface to cover said second oxide film; and

(c-2) diffusing said second impurity into said substrate from said second film.

19. A method of manufacturing a semiconductor device, comprising the steps of:

(a) preparing a substrate of a first conductivity type, having a first main surface and a second main surface which are opposed to each other;

(b) forming an impurity diffusion layer of a second conductivity type different from said first conductivity type by diffusing a first impurity into said substrate from said first main surface; and

(c) forming an impurity diffusion region of said second conductivity type by diffusing a second impurity into said substrate from part of said second main surface, to have a bottom surface reaching said impurity diffusion layer and surround a portion of said substrate which has said first conductivity type in a plan view,

wherein said portion surrounded by said impurity diffusion region is defined as an element formation region,

the method further comprising:

(d) forming a first impurity region of said second conductivity type partially in said second main surface in said element formation region;

(e) forming a second impurity region of said first conductivity type partially in said second main surface in said first impurity region; and

(f) forming a gate electrode on said second main surface with a gate insulating film interposed therebetween above said first impurity region positioned between said second impurity region and a portion of said substrate which has said first conductivity type,

wherein said first impurity region serves as a base of a transistor,

said second impurity region serves as an emitter of said transistor, and

said impurity diffusion layer serves as a collector of said transistor.

20. The method according to claim 19, further comprising the steps of:

(g) forming a first main electrode formed on said first main surface to be into contact with said impurity diffusion layer; and

(h) forming a second main electrode formed on said second main surface to be into contact with said first and second impurity regions.

21. The method according to claim 20, further comprising the step of:

(i) thinning said impurity diffusion layer by polishing said substrate from the side of said first main surface only by a predetermined film thickness,

wherein said step (i) is executed before said step (g).

22. The method according to claim 21, further comprising the step of:

(j) forming a local lifetime region by implanting an impurity into said portion of said substrate which has said first conductivity type from said side of said first main surface through said impurity diffusion layer,

wherein said step (j) is executed after said step (i).

23. The method according to claim 19, further comprising the step of:

(k) forming a first local lifetime region by implanting proton into a substantially middle region, with respect to a film thickness direction, of said portion of said substrate which has said first conductivity type, from said first main surface through said impurity

diffusion layer.

24. The method according to claim 23, further comprising the step of:

(l) forming a second local lifetime region by implanting helium into a deep region of said portion of said substrate which has said first conductivity type, said deep region being nearer to said impurity diffusion layer than said first local lifetime region.

25. A method of manufacturing a semiconductor device, comprising the steps of:

(a) preparing a substrate of a first conductivity type, having a first main surface and a second main surface which are opposed to each other;

(b) forming, in said first main surface, an impurity diffusion layer of a second conductivity type different from said first conductivity type, said impurity diffusion layer serving as a collector of a transistor; and

(c) forming, partially in said second main surface, an impurity diffusion region of said second conductivity type having a bottom surface reaching said impurity diffusion layer and surrounding a portion of said substrate which has said first conductivity type in a plan view,

wherein said portion surrounded by said impurity diffusion region is defined as an element formation region,

the method further comprising:

(d) forming, partially in said second main surface in said element formation region, a first impurity region of said second conductivity type serving as a base of said transistor;

(e) forming, partially in said second main surface in said first impurity region, a second impurity region of said first conductivity type serving as an emitter of said

transistor;

(f) forming a gate electrode on said second main surface with a gate insulating film interposed therebetween above said first impurity region positioned between said second impurity region and a portion of said substrate which has said first conductivity type; and

(g) forming a first local lifetime region by implanting proton into a substantially middle region, with respect to a film thickness direction, of said portion of said substrate which has said first conductivity type, from said first main surface through said impurity diffusion layer.

26. The method according to claim 25, further comprising the step of:

(h) forming a second local lifetime region by implanting helium into a deep region of said portion of said substrate which has said first conductivity type, said deep region being nearer to said impurity diffusion layer than said first local lifetime region.